

New Method for Making Very High Speed Time-Interleaved A/D Converters

Patent Title: Methods and Structures for Reconstruction of Substantially Uniform Samples from Substantially Nonuniform Samples

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This invention is concerned with methods and structures for reconstruction of uniform digital samples from nonuniform digital samples.

Market Opportunity

The ultimate goal of modern communication systems and advanced digital signal processing systems is to replace as many analog circuits as possible with digital ones in order to reduce size, cost and energy consumption. This has triggered an increasing demand for high-speed and high-resolution analog-to-digital converters (ADCs). Taking one of the leading producers of semiconductor devices, Analog Devices, Inc., as an example, their revenue for fiscal year 2009 approached \$2 billion [1], of which approximately 48% was derived from the sales of data converters. That percentage has grown steadily since 2003.

Our invention facilitates the efficient realization of time-interleaved (TI) ADCs, which is a promising approach to improve the sampling rate of existing analog-to-digital conversion techniques by utilizing M lower speed ADCs in parallel. It is envisioned that TI ADC will emerge as a prominent technique for high-speed data conversion as required in wireless communications, smart meters and other advanced applications.

The HKU Invention

In an M -channel TI ADC, M ADCs are operated in parallel so as to increase the effective sampling rate by a factor of M . However, any small timing mismatches between the M ADCs will cause a significant degradation in the resulting resolution [2]. Conventionally, the timing mismatch correction problem has been solved using the concept of a perfect reconstruction filter bank [3]. However, when the timing mismatch errors change during operation, say due to component variations, the correction filters have to be redesigned and a large number of expensive general-purpose multipliers is required to compensate for the new timing mismatch errors. Moreover, its implementation complexity increases exponentially with the number of channels, which prohibits the realization of very high-speed TI ADCs with a large number of channels.

Our invention overcomes the abovementioned limitations and reconstructs the desired uniform samples directly

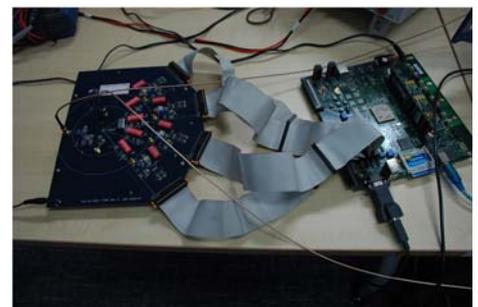


Fig.1: A 4-channel 12-bit 320MHz TI ADC prototype

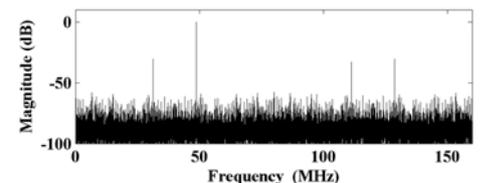


Fig.2: Input Signal

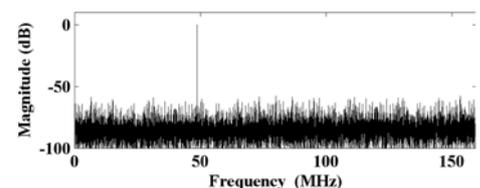


Fig. 3: Output Converges after 2 Iterations

from the nonuniform counterparts in an iterative manner. Important advantages are: 1) it enables the online adaptation of possible changing timing mismatch errors with few general-purpose multipliers, 2) its implementation complexity is independent of the number of channels, 3) only a few iterations is required for convergence to arbitrary resolution, and 4) it forms a framework for designing ADCs with different performance/complexity tradeoffs. As a result, this invention is more amenable to efficient real-time implementation of very high-speed and high-resolution TI ADCs. Fig 1 shows a 4-channel 12-bit 320MHz TI ADC prototype implemented using four AD9326 80Msps ADC chips. The prototype is able to remove the spiky noises due to timing mismatch in Fig 2 and converge by taking just two iterations, as shown in Fig 3.

About the Lead Inventor

Prof. S. C. Chan is a Professor at the Department of Electrical and Electronic Engineering of the University of Hong Kong. He was a visiting researcher at Microsoft Corporation, Redmond, USA, Microsoft, Beijing, China, University of Texas at Arlington and Nanyang Technological University, Singapore. His research interests include fast transform algorithms, filter design and realization, multirate and biomedical signal processing, communications and array signal processing, high-speed AD converter architecture, bioinformatics and image-based rendering. Prof. Chan is currently a member of the Digital Signal Processing Technical Committee of the IEEE Circuits and Systems Society, and is Associate Editor of IEEE Transactions on Circuits and Systems I and of the Journal of signal processing systems. He was Chairman of the IEEE Hong Kong Chapter of Signal Processing 2000-2002 and organizing committee member of IEEE ICASSP 2003 and ICIP 2010.

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